Remarks

This Amendment is responsive to the July 25, 2006 Office Action. Reexamination and reconsideration of claims 1-29 is respectfully requested.

Summary of The Office Action

Claims 1-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chevalier (US 5,898,634)(Chevalier) in view of Mori et al. (U.S. 6,891,214)(Mori) and further in view of Perner (U.S. 6,694,282)(Perner). No rationale has been provided for rejecting claims 7, 9, and 11, which were rejected in an omnibus rejection of claims 1-11.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §103

To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143.01 Second, there must be a reasonable expectation of success. MPEP 2143.02 Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, none of the first, second, or third criteria described in MPEP 2143.03 are satisfied. The combination of references does not teach or suggest all the claim limitations. Specifically, none of the references, alone and/or in combination, teach detecting input over-voltage conditions. Thus, none of the claims are obvious for at least this reason. Additionally, there is no motive to combine the references since Chevalier describes a real-time adaptive feedback loop while Mori and Perner are unrelated to real-time feedback. Furthermore, it is unlikely that the proposed combination could be built due to overwhelming

memory and space requirements and, if built, it likely could not provide the real-time adaptive feedback loop.

Mori

Mori describes storing over-current and over-temperature indications in a memory. C7, 14-53, C10, 130-35. The over-current condition is obtained by monitoring the output current of a switching element. Fig. 9, C7, 155-65. Mori is silent concerning storing input operations conditions.

Perner

Perner describes storing calibration data (e.g., lower calibration temperature, upper calibration temperature) in a PROM during fabrication or as read form an external location at some other time. C7, 137-62, C9 120-28. Perner is also silent concerning storing input operation conditions (e.g., input voltage, Vcc)

In prior prosecution Mori and Perner were shown to be inadequate, thus the Office Action has added Chevalier.

Chevalier

Chevalier discloses an integrated circuit with a supply voltage detection circuit (200) that produces an output that indicates a voltage range of the supply range. The output can be used in a feedback loop to adjust operation of the integrated circuit. (Abstract) The output may be a multiple bit code that identifies a supply voltage. The device also includes a status register latch for storing the multiple bit output signal. C1, 151-52. While Chevalier describes detecting a supply voltage, it simply reports this voltage, does not compare it to any "acceptable" value, and thus does not detect any out of specification condition. Consider C4, 19-11, which reads "it may be desired to use a look up table for comparing output from the supply voltage detection circuit with recorded data to determine an operating voltage." This indicates that Chevalier is merely viewing the output signal from the detector in light of known reference values (e.g., 2.7V, 3.0V), to facilitate calibrating a voltage sensor to account

for variations in a manufacturing process. However, this has nothing to do with detecting and/or recording an over-voltage condition because there is no comparison to any "good" or "good range" of values. The voltage is simply detected and temporarily stored in a latch register.

While the output signal can be compared to values in the lookup table, this isn't used to detect an out of specification condition but rather as part of a feedback loop that will "adjust the operation of the integrated circuit in response to the detected supply voltage range." C5, l67 to C6, l8. The output can be stored in a latch, but the output is not data related to or describing an out of specification condition but rather is a simple description of the currently detected voltage without any out of specification property associated with or related to the value.

So, Chevalier does not disclose detecting an over-voltage condition on any input and thus, it follows, also does not disclose recording any over-voltage condition. Chevalier simply detects and reports on a voltage range, completely disregarding whether the detected range is inside or outside a desired range.

The Office Action is incorrect when it asserts that "in reflect of the Vref of the IC is 2 volts, and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)". This argument does not indicate that Chevalier discloses detecting an over voltage condition because the 2 volts given as an example is an example of an operating range for the integrated circuit for which calibration is data stored, not of an error (e.g., over voltage) condition. Furthermore, even if the 2 volts was outside a desired range, there is nothing in Chevalier that could detect or respond to that condition. For at least these reasons all the claims are not obvious over Chevalier, Mori, and Perner.

Official Notice

MPEP §2144.03 speaks directly to "Official Notice". This section counsels that only "in limited circumstances is it appropriate for an examiner to take official notice of facts not in the record or to rely on 'common knowledge' in making a rejection." MPEP §2144.03 This section specifically warns that "such rejections should be judiciously applied." MPEP §2144.03 Applying "Official Notice" to reject 23 of 29 claims is not "judiciously applying"

this technique. Furthermore, the items that are officially noticed are not so generally well known or applicable as indicated in the Office Action. For example, the Office Action asserts that it would be obvious to use the PROM memory of Perner with Chevalier. However, this combination could not actually be built because it would quickly consume all the PROM memory in existence, would achieve unimaginable physical dimensions, and would produce a machine unsuited to the real-time feedback loop of Chevalier. Thus, official notice is poorly taken here. For this additional reason these obviousness rejections are improper and should be removed.

Claims will now be discussed individually.

Claims 12, 17-18, 21-22, and 26 were rejected using the same rationale, that in Chevalier "the detected variation input voltage range constitute of over-voltage conditions, in reflect of the Vref of the IC is 2 volts [see col. 1, lines 11-17, and col. 5, lines 40-67], and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)".

This quoted rationale is somewhat difficult to understand, which denies Applicant a meaningful opportunity to reply. What is clear, however, is that Chevalier is simply reporting on a detected voltage. The voltage described (e.g., Vref = 2 volts) is inside an operating range and used either for calibration or for a feedback loop, not for error detecting. A code for the detected voltage may be stored temporarily in a high-speed memory (e.g., register) to support the adaptive feedback loop. The code may be used to adapt an operating setting of the integrated circuit from which the voltage was detected. But no error condition is detected or stored.

The Office Action uses Mori and Perner to establish that the voltage code could be stored in a permanent memory. No-one skilled in the art would be motivated to store the voltage detected in Chevalier in a slow permanent memory because the voltage code is used as part of a substantially instantaneous feedback loop and is then discarded. The detected voltage is constantly being overwritten. Burning a PROM or fuse would make the feedback loop in Chevalier too slow for practical use and would quickly consume inordinate amounts

of memory with useless data. Imagine how many fuses would be burned in just one second of operation of the Chevalier/Mori/Perner combination. If the system operated at 100 MHz, then 100 million fuses would be burned or 100 million PROM locations would be forever altered in just one second. And all those fuses and PROM locations would store irrelevant information that would never be consulted because the combination would have moved on in its real-time adaptive feedback loop to look at the next voltage, not at any previous voltage.

Clearly the Chevalier/Mori/Perner combination is impractical at best, impossible to construct at worst, and worthless for any task if constructed. For at least these reasons the claims are not obvious and are in condition for allowance.

Claim 13

This claim depends from claim 12, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally this claim recites filtering an input operational voltage for at least a duration of one clock period, which the Office Action asserts would have been obvious to add. The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 19

This claim depends from claim 18, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally this claim recites a filter module, which the Office Action asserts would have been obvious to add. The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 14

This claim depends from claim 12, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally this claim recites only recording the over-voltage condition if the operational voltage exceeds the specified voltage by a selected amount, which the Office Action asserts would have been obvious to add. The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 15

This claim depends from claim 14, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally this claim recites only recording the over-voltage condition if the operational voltage exceeds the specified voltage by at least two times an expected noise voltage value, which the Office Action asserts would have been obvious to add. The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. Additionally, the rationale provided concerns the limitation in claim 14, not the additional limitation in claim 15. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 16

This claim depends from claim 12, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally this claim recites verifying recordation of the input operating over-voltage condition, which the Office Action asserts would have been obvious to add. The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. No motive could possibly be found for verifying the recordation in the Chevalier/Mori/Perner combination since the combination describes a real-

time adaptive feedback loop. Verifying the recordation would likely slow down the feedback loop so much that the instantaneous adaptation would be lost, rendering the machine worthless for its appointed task. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 23

This claim depends from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance.

Claim 28

This claim depends indirectly from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance.

Claim 24

This claim depends from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance.

Claim 25

This claim depends from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance.

Claim 27

This claim depends from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance.

Claim 29

This claim depends from claim 22, which has been shown to be not obvious. Thus, this claim is similarly not obvious and is in condition for allowance. Additionally this claim recites that the system includes a BIOS to determine the selected number of out-of-specification input operational conditions to detect. The Office Action simply asserts that

Mori discloses a BIOS. Simply have a BIOS does not mean that the BIOS is configured to determine the number of out-of-specification conditions to detect. Neither Mori nor any of the other references teach this element. For this additional reason this claim is not obvious and is condition for allowance.

Claims 1-11

These claims were rejected with the following rationale: "[t]he claimed method steps are interpreted and rejected as rejection stated above." Once again this rationale is somewhat difficult to understand leaving the Applicant with a less than meaningful opportunity to reply. Notwithstanding the deficiency in the rejection, Applicant once again can reply that the Chevalier/Mori/Perner combination does not teach each and every limitation found in independent claims 1 and 4. For example, none of the combinations, alone and/or in combination, teach storing data concerning an over-voltage condition in an indelible memory (claim 1) or comparing an input operational condition with a specified condition (claim 4). The only thing stored in Chevalier is an instantaneous voltage reading, which is completely unrelated to any error condition and which is discarded as soon as it is used in the adaptive real-time feedback loop. Additionally, the arguments concerning the fact that the combination of Chevalier/Mori/Perner likely could not be built and if built would be inoperative for its assigned task apply equally here. Thus, these claims are not obvious over the references and are in condition for allowance.

Additionally, some of the claims in the set of claims 1–11 include elements or limitations not found in claims 12-29. Thus, this omnibus rejection actually provides no rejection for at least claims 7, 9, and 11.

For example, claim 7 includes the limitation that the specified amount of time is associated with a power on reset time. None of the references describe this limitation and none of the claims 12-29 describe this limitation. Thus, there is no rationale provided for rejecting claim 7. Similarly, claim 9 includes recording a clock speed. Not only do none of the references describe recording a clock speed, but none of claims 12-29 describe storing a clock speed. Thus, there is no rationale provided for rejecting claim 9. Likewise, claim 11 recites reading a signature value stored in an indelible memory. None of the references

describe this element and none of the claims 12-29 describe this element. Thus there is no rationale for rejecting claim 11. For at least these additional reasons, claims 7, 9, and 11 have not even been rejected once and remain unobvious and in condition for allowance. No rejection can be made final concerning at least these claims.

Conclusion

For the reasons set forth above, claims 1-29 patentably and unobviously distinguish over the references and are allowable. Additionally, no rationale has been provided for rejecting claims 7, 9, and 11. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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